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## ABSTRACT OF THE DISCLOSURE

A carrier lock detector for a QPSK or 4-QAM system implements a lock detection algorithm that maps detected signals onto one of first and second areas associated with  $(I, \oplus I_3) \cdot (Q, \oplus Q_3)$ states defined by  $\overline{Q_1 \oplus Q_2} \cdot (I_1 \overline{I_2} \overline{I_3} + \overline{I_1} I_2 I_3) + (\overline{I_1 \oplus I_2}) \cdot (Q_1 \overline{Q_2} \overline{Q_3} + \overline{Q_1} Q_2 Q_3)$ , or alternatively,  $(\overline{I_1 \oplus I_2} \cdot \overline{Q_2 \oplus Q_3}) + (\overline{Q_1 \oplus Q_2} \cdot \overline{I_2 \oplus I_3})$ , respectively. When detected signals map onto one of the first areas, a first signal is generated. When detected signals map onto one of the second areas, a second signal is generated. difference between the first and second signals exceeds a threshold, a carrier lock detection signal is generated to enable a decoder. The carrier lock detector is able to detect carrier lock at a raw BER of 1e-2 or greater at a. very low signal-to-noise ratio.